Midterm Test # 2 Solution

Q1-(30pts)

Signed & Unsigned Multiplication and Division

a) Multiply X (Multiplicand) = 11_2 to Y(Multiplier) = 11011_2, *use one of the sequential unsigned multiplier versions* ***(5pts)***. How many registers are required, what are their sizes, and what do they hold? ***(3pts)***. How large an ALU is required? ***(2pts)***.

Note (X and Y are 5-bit signed numbers in 2's complement representation).

المطلوب في هذا السؤال هو استخدام أحد طرق الضرب بدون إشارة لضرب العددين

$X=MC=11_2$ $Y=MR=11011_2$

وقد تم التنويه في الملاحظة على أن العددين X & Y، هما عددين بحجم 5 بت ومتمثلين في التمثيل 2's complement،
فهذا يتطلب منك أن تقوم بتجريد العددين من الإشارة لكي تستخدم عملية الضرب بدون إشارة،

العدد الآول: $X=11_2$ هذا العدد عبارة عن 00011_2 بالنسبة ل 5 بت يكون العدد موجب ويساوي +3

العدد الثاني: $Y=11011_2$ هذا العدد بالنسبة ل 5 بت يكون العدد سالب فنقوم بتحويله إلى عدد بالاشارة ويكون

Y=-(00101) = -5

فيتم تجريد الرقم من الاشارة وتستخدم أحدى الطرق المعروفة للضرب بدون إشارة التي درسناها وهم

1st version unsigned multiplication
2nd version unsigned multiplication
3rd version unsigned multiplication

بعد عملية الضرب رح يصبح الناتج

PR=00000 0 1111 = 15

تقوم بوضع الإشارة وتصبح النتيجة

-15

How many registers are required, what are their sizes, and what do they hold? ***(3pts)***. How large an ALU is required? ***(2pts)***.

هنا الإجابة تكون على حسب الفيرجن الذي استخدمته ويجب أن تكون الإجابة إيضا مطابقة لحجم الملتيبلاير 5 بت

- 1st version unsigned multiplication:
  Three registers.
  MC and PR registers are 10 bits. hold Multiplicand and Product.
  MR register is 5 bits. holds multiplier.
  ALU size = 10 bits.
- 2nd version unsigned multiplication
  Three Registers
  MC and MR registers are 5 bits hold Multiplicand and Multiplier.
  PR register is 5 bits holds Product.
  ALU size = 5 bits.
- 3rd version unsigned multiplication
  Two Registers.
  MC register size = 5 bits holds Multiplicand.
  PR register size = 5 bits holds Product.
  ALU size = 5 bits.

b) Divide X (Dividend) = 10011_2 by Y(Divisor) = 1011_2, *use one of the sequential divider versions* ***(5pts)***. How many registers are required, what are their sizes, and what do they hold? ***(3pts)***. How large an ALU is required? ***(2pts)***.
Note (X and Y are 5-bit signed numbers in 2's complement representation).

نفس فكرة الفقرة السابقة اتدير تشيك على الارقام وتشوفهم لو سالب اتحول العدد لموجب واتدير عملية القسمة وبعدين تضع الاشارة كالتالي

X= 10011 = -(01101)= -13
Y= 01011 = + 11
-13/11
Q sign = Div sign --> Q = -1
Rem sign = Div sign xor Dr sign = - xor + = 1 xor 0 =1 --> Rem sign is -ve
Rem = -2
للتأكيد
Div = Q * DR + Rem
Div = -1 * 11 + -2 = -13
بالنسبة للفقرة الآخرى

How many registers are required, what are their sizes, and what do they hold? ***(3pts)***. How large an ALU is required? ***(2pts)***.

1st version
Three Registers
DR and Rem resgiters 10 bits
Q register 5 bits
ALU 10 bit
3rd Version
Two Registers
DR register 5 bit
Q and Rem in the same register = 10 bits
ALU 5 bits

c) How many adders (Half and Full) are required to implement a 2bit × 2bit array signed multiplication using Bough Wooley's method? ***(6pts)***. Calculate the longest gate delay in the carry path***(4pts)***.

لكي نعرف كم عدد الفل آدر والهالف آدر لابد من تطبيق خطوات الطريقة ومن ثم رسمها
بالنسبة للطريقة أخذناها ل 4 بت فبالتالي رح اتكون بسيطة لل 2 بت
الصورة النهائية للمعادلة ستكون كالتالي

$$\begin{array}{llll} & & \overline{X1Y0} & X0Y0 \\ + & X1Y1 & \overline{X0Y1} & \\ + & 1 \quad 1 & & \end{array}$$

Z3 Z2 Z1 Z0

بعد الرسم يتضح أن سنتحصل على
1 Full Adder, 2 Half Adder
Gate Delay in the longest carry path = 7 Gate Delay

Q2-(25pts)

Floating Point Arithmetic

a) Represent $(-1101.011 \times 2^{-130})$ in IEEE-754 single precession format. ***(5pts)***

Single Precession Format S = 1, E = 8, F= 23 bit

$-1101.011 \times 2^{-130} = -1.101011 \times 2^{-127}$

Val(E)= E-127 --> Val(E) = -127= E - 127 --> E = 0

بما إن E=0 فإننا لا نستطيع تمثيل هذا العدد في هذه الفورمات لان لما E=0 تعتبر حالة خاصة

فنحاول أن نمثل العدد على أساس أنه Denormalized

Denormalized format $(-1)^S \times 0.F \times 2^{-126}$

وهذا العدد عند تحويله ل Denormalized

$-1.101011 \times 2^{-127} = -0.1101011 \times 2^{-126}$

∴ نستطيع تمثيل هذا العدد على أساس أنه Denormalized Number

S=1 E=0 F=1101011

1 0000 0000 1101 0110 0000 0000 0000 000

b) Consider A and B are floating point numbers in (S^1,E^3,F^6) format. $A=1.001\times2^{-2}$ and B=1.11101. Perform the following operations, round the result to the nearest even, and then represent the result in (S^1,E^3,F^6) format. What is the decimal value of the result according to this format (S^1,E^3,F^6).

i. A + B ***(10pts)***

النتيجة

0 100 000110

Decimal Value 2.1875

حاولوا اتجاوبوا الخطوات بروحكم

ii. A × B ***(10pts)***

النتيجة

0 010 000100

Decimal Value 0.53125

حاولوا اتجاوبوا الخطوات بروحكم

Q3-(20pts)

Performance

You are going to enhance a computer, and there are two possible improvements: either make multiply instructions run four times faster than before with speedup 1.15, or make memory access instructions run two times faster than before. The performance for multiplication hardware before improvement is 5×10^{-2} per second. and for memory access instructions is 2.5×10^{-2} per second.

If you improve Multiplication hardware the speedup =E= 1.15

E = Ex_time before/ Ex_time with enhancement

Multiplication Performance = 5×10^{-2} -->

Ex_time for multiplication = 1/ Multiplication Performance

Ex_time for multiplication = 20 sec

Ex_time for memory access = 40 sec

i. What is the overall execution time before improvement. ***(5pts)***
1.15 = Ex_Time Before /((Ex_Time Before - f1) + f1/4)
1.15 = Ex_Time Before /((Ex_Time Before - 20) + 20/4)
Ex_Time Before = 115 sec

ii. What is the overall execution time if you improve only multiplication? ***(5pts)***
Ex_Time with multiplication enhancement = Ex_time before/ Speedup
=115/1.15 = 100 sec

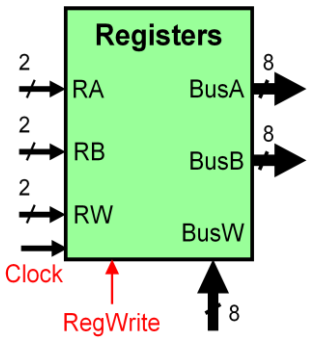
iii. What will the speedup be if you improve only memory access?***(5pts)***
E = 115 / ((115-40) + 40/2)
E = 1.2015

iv. What will the speedup be if both improvements are made? ***(5pts)***
E = 115/ ((115-40-20)+ 40/2 + 20/4)
E = 1.4375

Q4-(25pts)

Single Cycle Datapath and Control

a) Draw the hardware of the register file shown below. ***(10pts)***



حل هذه الفقرة هو نفس الرسم الموجود في السلايد
CH5_5.1_5.4_P2.ppt slide 7
ولكن هنا حجم الديكودر 2:4
وحجم الريجستر هو 8 بت

b) Consider the following single-cycle datapath for the MIPS processor implementing a subset of the instruction set (R-Type, Immediate Arithmetic and Logic, LW/SW, jump and branch instructions). If the following signals have a stuck at 0 or 1. Which instructions mentioned above will not work correctly? Explain why.

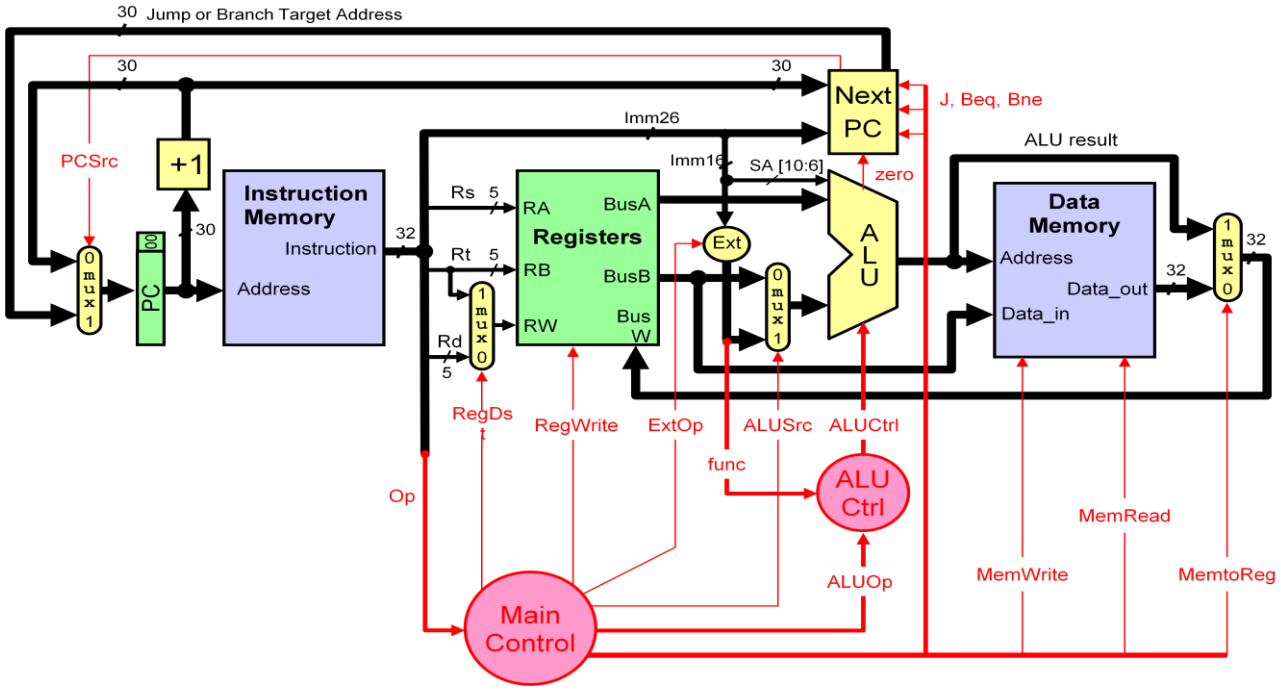
i. RegDst stuck at 0. ***(5pts)***
Immediate Arithmetic/Logic and LW instructions will not work correctly because the destination register should be chosen depended on 5-bit rt.

ii. ALUSrc stuck at 1. ***(5pts)***

R-type and Branch instructions will not work correctly because busB is need to be as input to the ALU to perform these instructions.

iii. MemToReg stuck at 1. ***(5pts)***

LW instruction will not work correctly because we need to store the Data_out from data memory to the destination register.



Optional Question *(25% of the mark obtained).*

What is the dynamic range and the special cases representation for IEEE-754 half precession format.

الحلول المطلوبة كالتالي

Half Precession S=1 E=5 F=10

كتابة قيمة مايلي حتى ولو بالشكل

0 00000 0000000000 = +ve zero

Largest +ve Normalized Number

Smallest +ve Normalized Number

Largest +ve De-Normalized Number

Smallest -ve De-Normalized Number

Largest -ve Normalized Number

Smallest -ve Normalized Number

Largest -ve De-Normalized Number

Smallest -ve De-Normalized Number

Special Cases Nan -zero +zero -∞ + ∞